REMARKS/ARGUMENTS

These remarks are in response to the Office Action dated August 4, 2005. Claims 1-21 are currently pending.

Allowable Subject Matter and New Claims

The Examiner indicates that claims 4, 5, 8-12 and 14-18 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the Examiner's indication.

Claim Rejections

In the Office Action, the Examiner rejected claims 1-3, 6, 7, 13 and 19 under 35 U.S.C. §103(a) as being unpatentable over Doblar et al. (U.S. Patent No. 6,338,144) in view of Rai (U.S. Patent No. 6,529,036). In so doing, the Examiner stated:

> In claim 1, Doblar et al. teaches all claimed features in Figs. 1-2, a method comprising: buffering a differential clock signal (Ck,/Ck) with a single buffer circuit (26a) for a plurality of load circuits (20a-20c); with the exception of teaching the step of configuring the single buffer circuit to adjust to alterations in the number of load ircuits receiving the differential clock signal, wherein noise immunity is increased. However, Rai teaches in Fig. 6, a step of configuring the single buffer circuit (104) to adjust to alterations in the number of load circuits (load circuits would be coupled to outputs 228 and 230) receiving the differential clock signal, wherein noise immunity is increased.
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> In claim 2, Rai further teaches the method of claim 1 wherein buffering further comprises buffering the differential clock signal (CLK, CLKB) with a differential amplifier circuit (202) including a programmable impedance circuit (234, 236) and a programmable current source circuit (200, 204).
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> In claim 3, Rai further teaches the method of claim 2 wherein configuring the single buffer circuit further comprises adjusting (232) an impedance level of the programmable impedance circuit (234, 236) and adjusting (100, 112) a current source level of the programmable current source circuit (200, 204).
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> In claim 6, Doblar et al. teaches all claimed features in Figs. 1-2, a circuit comprising: a clock signal source (12) providing a differential clock signal (Ck, /Ck); and a configurable buffer circuit (26a) for receiving the differential clock signal and providing a clock signal output for a plurality of load circuits (20a-20c), with the exception of teaching wherein the configurable buffer circuit achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable

> buffer circuit, wherein noise immunity is increased. However, Rai teaches all claimed features in Fig. 6 a configurable buffer circuit (104) achieves a constant bandwidth (matched impedance results in constant bandwidth) and voltage level (col. 1, line 47) for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit, wherein noise immunity is increased.
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> In claim 7, Rai further teaches the circuit of claim 6 wherein the configurable buffer circuit further comprises a differential amplifier circuit (202) including a programmable output impedance circuit (234, 236) and a programmable current source circuit (200, 204).

Applicants respectfully disagree.

The present invention is directed to increasing noise immunity for clocking signals in high speed digital systems. Referring to Figure 2 of the present invention, clock buffering in accordance with the present invention utilizes a single clock source 20, and *a single buffer circuit* 22, where the single buffer circuit 22 is configurable and controlled via an impedance/current control circuit 24 for N number of load circuits 26a, 26b, ... 26n. According to the present invention, the single buffer circuit 22 includes a differential amplifier that has a programmable output impedance and a programmable current source controlled by control signals of the impedance/current control circuit (see FIG. 3). By adjusting the programmable current source and output impedance together, a constant output voltage from the differential amplifier circuit can be achieved regardless of the number of load circuits. Because the present invention does not utilize multiple stages of serial buffering, the number of load circuits receiving the clock signal can be increased as desired without increasing the noise.

While Doblar is also directed to increasing noise immunity, Doblar does so in a completely different manner. In Doblar, *a plurality of buffer circuits 26a-26d* are used to pass the differential clock signal to the plurality of load circuits 20a-20c. As is seen in FIG. 2 of Doblar, the fanout buffer 16 includes *several* buffer circuits 26a-26d that distribute the differential clock signal to the various memory modules 20a-20c. According to Doblar, each buffer circuit 26 includes emitter-coupled logic (ECL) circuits. By utilizing ECL circuits in each

buffer circuit 26, noised immunity is improved when the ECL circuits are used in differential mode. (Col. 6, lines 1-28). As is shown in FIG. 2 of Doblar, each memory module 20a-20c is associated with a buffer circuit 26b-26d, and each buffer circuit 26a-26d is configured like the rest (FIG. 3). Accordingly, if a new memory module 20 is added, it too would be associated with its own buffer circuit 26.

Rai, on the other hand, is directed to a circuit that maintains constant voltage output levels independent of process corner and temperature variation. In Rai, a driver circuit (FIG. 4, item 104) is configured to match the impedance of a transmission line (TL1, TL2) thereby reducing sensitivity of a swing in voltage levels between output pins (228, 230) to variations in a load resistor (RL). (Column 2, lines 24-33).

Applicants respectfully submit that both Doblar and Rai fail to teach or suggest "buffering a differential clock signal with a single buffer circuit for a plurality of load circuits and configuring the single buffer circuit to adjust to alterations in the number of load circuits," as recited in claim 1. In the present invention, the single buffer circuit (FIG. 2, item 22) provides the differential clock signal to the plurality of load circuits. By using a single buffer circuit, as opposed to several in series, the number of load circuits can be increased without increasing signal noise.

In Doblar, FIG. 2 shows that the fanout buffer 16 includes a plurality of buffer circuits 26a-26d, as opposed to "a single buffer circuit." There is no teaching or suggestion that any of the buffer circuits 26 is configured to adjust to alterations in the number of load circuits because, as is shown in FIG. 2, each memory module 20a-20c is associated with a buffer circuit 26b-26d, and each buffer circuit 26a-26d is configured like the rest (FIG. 3). Accordingly, if a new memory module 20 is added, it too would be associated with its own buffer circuit 26, and none of the buffer circuits 26 would need to be adjusted. In Rai, the driver circuit shown in FIG. 6 and

described in column 4, line 49 to column 6, line 67, is not configured to "adjust to alterations in the number of load circuits." Rather, Rai only speaks to maintaining constant voltage output levels across process corner and temperature. Rai mentions that the driver circuit 104 can match impedance of a transmission line by choosing R1_0 and R2_0 to have the same value as the transmission line impedance. While this reduces swing sensitivity to variations of a load resistor value, there is no teaching or suggestion of "configuring the signal buffer circuit to adjust to alterations in the number of load circuits receiving the differential clock signal," as recited in claim 1.

In addition, both Doblar and Rai fail to teach or suggest a configurable buffer circuit that "achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit," as recited in claim 6. In Doblar, nothing teaches or suggests that the buffer circuits 26 are configured to make adjustments based on the number of load circuits coupled to it. Similarly, although Rai mentions maintaining the voltage output while varying load resistance (impedance), Rai does not teach or suggest varying the number of load circuits.

Finally, both Doblar and Rai fail to teach or suggest a buffer circuit comprising a differential amplifier circuit including a "programmable impedance circuit" to provide a constant bandwidth and voltage level for a differential output clock signal, as recited in claim 13 and claim 19. In the Office Action, the Examiner states that Rai's driver circuit 104 has this feature in FIG. 6. In particular, the Examiner indicates that Rai's sections 234 and 226 teach the present invention's programmable impedance circuit. Applicants respectfully disagree. Rai's sections 234 and 226 (described at column 5, lines 26-48) simply set the output common-mode voltage. In contrast to the present invention, the output impedance of the circuit is strictly set by the

values of R1_0 and R2_0. Because the values of R1_0 and R2_0 are generally fixed, they do not teach or suggest a programmable impedance circuit, as recited in claim 13 and claim 19.

For the foregoing reasons, Applicants respectfully submit that claims 1, 6, 13 and 19 are allowable over Doblar in view of Rai. Claims 2-5, 7-12 and 14-18 depend from claim 1, 6 and 13, respectively, and for that reason are also allowable.

Conclusion

In view of the foregoing, Applicants submit that claims 1-21 are allowable. Applicants respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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Date

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